WHAT IS CLAIMED IS:

1. A processing system comprising:

a processor configured to

formulate an instruction and data for sending to a device, said instruction requesting the device to perform a command and return data to the processor; and

a bus controller configured to

generate a system bus operation to send the formulated instruction and data along with a thread identifier to the device.

2. The processing system of claim 1, wherein the device is a table lookup unit.

3. The processing system of claim 1, wherein the bus controller is further configured to receive the device return data from a system bus along with the thread identifier.

4. A processor that executes instructions in threads, said processor comprising:

a context register file having a separate set of general registers for a plurality of contexts, wherein said threads are each assigned a separate context; and

context control registers having a separate set of control registers for the plurality of contexts.

5. The processor of claim 4, wherein the context register file includes 32 general registers for 8 contexts.

6. The processor of claim 4, wherein the context register file includes for each context:

a context program counter;

a context status register; and

a write address register.

7. The processor of claim 6, wherein the context program counter holds a program counter pointing to a next instruction in an associated context.

8. The processor of claim 6, wherein the context status register holds data that indicates whether an associated context is awaiting data from an external source.

9. The processor of claim 6, wherein the write address register stores an address of a register associated with a context that is awaiting data.

10. The processor of claim 6 further including:

a scheduler configured to select a context to activate.

11. The processor of claim 10 further including:

means for receiving a context switch instruction;

means for receiving an identifier of a next context to activate from the scheduler;

means for performing a next instruction in a current context; and

means for pointing a processor program counter to the context program counter in the context control register associated with the next context.

12. A processing system comprising:

a processor configured to

formulate an instruction and data, from a thread associated with a first context, for sending to a device, said instruction requesting the device to perform a command and return data to the processor;

perform a context switch to switch from processing the first context to a second context; and

a bus controller configured to

generate a system bus operation to send the formulated instruction and data along with a thread identifier to the device.

13. The processing system of claim 12, wherein the processor is further configured to store an address of a destination register associated with the first context receiving the return data.

14. The processing system of claim 13, wherein the bus controller is further configured to receive the device return data from a system bus along with the thread identifier.

15. The processing system of claim 14, wherein said processor is configured to

write the return data to the stored destination register associated with the first context; and

clear a wait bit in a status register associated with the first context.

16. The processing system of claim 12, wherein the device is a table lookup unit.

17. The processing system of claim 12 said processor further including:

a context register file having a separate set of general registers for the first and second contexts; and

context control registers having a separate set of control registers for the first and second contexts.

18. The processing system of claim 17, wherein the context register file includes 32 general registers for the each context.

19. The processing system of claim 17, wherein the context register file includes for each context:

a context program counter;

a context status register; and

a write address register.

20. The processing system of claim 19, wherein the context program counter holds a program counter pointing to a next instruction in an associated context.

21. The processing system of claim 19, wherein the context status register holds data that indicates whether an associated context is awaiting data from an external source.

22. The processing system of claim 19, wherein the write address register stores an address of a register associated with a context awaiting data.

23. The processing system of claim 19 further including:

a scheduler configured to select the second context to activate.

24. The processing system of claim 23 further including

means for receiving an identifier of the second context to activate from the scheduler;

means for performing a next instruction in the first context; and

means for pointing a processor program counter to the context program counter in the context control register associated with the second context.

25. A method for processing a single instruction that both requests a system device operation and requests the system device return data, said method comprising the steps of:

fetching an instruction from memory;

forming a descriptor;

constructing a system bus address;

initiating a system bus operation to request a device to perform an operation and return data to a processor identified in a thread identifier; and

retrieving return data from a system bus based on the thread identifier provided with the returned data.

26. A method for switching between contexts using a processor having a context register file having a separate set of general registers for a plurality of contexts, each et of registers associated with a thread, and context control registers having a separate set of control registers for the plurality of contexts, said method comprising the steps of:

receiving a context switch instruction;

receiving an identifier of a next context to activate from the scheduler;

performing a next instruction in a current context; and

pointing a processor program counter to the context program counter in the context control register associated with the next context.